# SOLID-STATE IMAGING DEVICE AND ELECTRONIC APPARATUS

## CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 15/079,599, filed Mar. 24, 2016, which is a continuation of U.S. patent application Ser. No. 14/857,535, filed Sep. 17, 2015, which is a continuation of U.S. patent application Ser. No. 14/564,750, filed Dec. 9, 2014, now U.S. Pat. No. 9,179,082, which is a continuation of U.S. patent application Ser. No. 14/107,839, filed Dec. 16, 2013, now U.S. Pat. No. 9,049,392, which is a division of U.S. patent application Ser. No. 13/609,596, filed Sep. 11, 2012, now U.S. Pat. No. 8,638,382, which is a division of U.S. patent application Ser. No. 12/684,445, filed Jan. 8, 2010, now U.S. Pat. No. 8,314,870, which claims priority to Japanese Patent Application Serial No. JP 2009-006892, filed in the Japan Patent Office on Jan. 15, 2009, the entire disclosures of which are hereby incorporated herein by reference.

## BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an MOS Si substrate and an electronic apparatus, such as a camera, having the solid-state imaging device.

2. Description of the Related Art

Amplification-type solid-state imaging devices represented by MOS image sensors such as CMOS (complementary metal oxide semiconductor) image sensors are known as one type of solid-state imaging devices. Moreover, charge transfer-type solid-state imaging devices represented by CCD (charge coupled device) image sensors are also known. These solid-state imaging devices are broadly used in digital cameras, digital video cameras, and the like. In recent years, as solid-state imaging devices which are mounted on mobile apparatuses, such as camera-incorporated mobile phones or PDAs (personal digital assistants), the MOS image sensors have been used more than the CCD image sensors because the CMOS image sensors are advantageous in terms of lower power supply voltage, smaller power consumption, and the like.

An MOS solid-state imaging device has a configuration in which a plurality of pixels is arranged in a two-dimensional array, wherein each pixel is composed of a photodiode serving as a photoelectric conversion unit and a plurality of pixel transistors. In recent years, with the miniaturization of pixels, in order to reduce the area occupied by the pixel transistors per pixel, a so-called multi-pixel sharing structure is proposed in which a part of the pixel transistors is shared by a plurality of pixels. For example, Japanese Unexamined Patent Application Publication Nos. 2004/172950, 2006/054276, and 2006/157953 describe a solid-state imaging device with 2-pixel sharing structure.

## SUMMARY OF THE INVENTION

However, in MOS solid-state imaging devices, it is desirable to achieve a further increase in resolution by miniaturizing the pixels further. However, a further miniaturization of the pixels may lead to a reduction in the aperture area of a light receiving portion and thus sensitivity decreases. Therefore, it is desirable to achieve improvement in sensitivity even when pixels are miniaturized.



It is therefore desirable to provide a solid-state imaging device capable of achieving improvement in sensitivity even when pixels are miniaturized and an electronic apparatus having such a solid-state imaging device.

According to an embodiment of the present invention, there is provided a solid-state imaging device having a layout in which one sharing unit includes an array of photodiodes of 2 pixels by 4×n pixels (where, n is a positive integer), respectively, in horizontal and vertical directions.

In the solid-state imaging device according to the embodiment of the present invention, since one sharing unit includes an array of photodiodes of 2 pixels by 4×n pixels (where, n is a positive integer), respectively, in horizontal and vertical directions, the number of pixel transistors per pixel can be decreased, and thus the aperture area of each of the photodiodes can be increased. Moreover, since one sharing unit includes an array of photodiodes of 2 pixels by 4×n pixels, respectively, in horizontal and vertical directions, the readout wirings can be arranged independently for each pixel, and thus pixel addition can be performed within the floating diffusions. Furthermore, it is possible to decrease the area of the column signal processing circuit.

According to another embodiment of the present invention, there is provided an electronic apparatus including: a solid-state imaging device; an optical system that guides incident light to photodiodes of the solid-state imaging device; and a signal processing circuit that processes output signals from the solid-state imaging device. The solid-state imaging device has a layout in which one sharing unit includes an array of photodiodes of 2 pixels by 4×n pixels (where, n is a positive integer), respectively, in horizontal and vertical directions.

Since the electronic apparatus according to the embodiment of the present invention includes the solid-state imaging device, the number of pixel transistors per pixel can be decreased, and thus the aperture area of each of the photodiodes can be increased. Moreover, since one sharing unit includes an array of photodiodes of 2 pixels by 4×n pixels, respectively, in horizontal and vertical directions, the pixel addition can be performed within the floating diffusions, and the area of the column signal processing circuit can be reduced.

According to the solid-state imaging device of the embodiment of the present invention, since the aperture area of the photodiode can be increased, it is possible to achieve improvement in sensitivity even when the pixels are miniaturized.

According to the electronic apparatus of the embodiment of the present invention, since the aperture area of the photodiode in the solid-state imaging device can be increased, it is possible to achieve improvement in sensitivity even when the pixels are miniaturized. Therefore, it is possible to provide a high-quality electronic apparatus.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic diagram illustrating an exemplary configuration of a solid-state imaging device according to an embodiment of the present invention.

FIG. **2** is a layout diagram of one sharing unit in a pixel portion of a solid-state imaging device according to Embodiment 1.

FIGS. **3**A to **3**C are exploded planar layout diagrams of one sharing unit according to Embodiment 1.

FIG. **4** is a schematic cross-sectional view of an example of a two-layer wiring structure of Embodiment 1.